




Product Specification

AU OPTRONICS CORPORATION

(✓) Preliminary Specifications

() Final Specifications

| | |
|--|--|
| Module | 17.3"(17.25") FHD 16:9 Color TFT-LCD with LED Backlight design |
| Model Name | B173HW02 V1 (H/W:0A) |
| Note () | <i>LED Backlight with driving circuit design</i> |

Customer

Date

Checked &
Approved by

Date

Note: This Specification is subject to change without notice.

Approved by

Date

Prepared by

Date

NBBU Marketing Division
AU Optronics corporation



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Record of Revision

| Version and Date | Page | Old description | New Description | Remark |
|------------------|------|---------------------|-----------------|--------|
| 0.1 2011/4/27 | All | Preliminary Edition | | |
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1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentarily. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.



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2. General Description

B173HW02 V1 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the FHD 16:9 1920(H) x 1080(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are LVDS interface compatible.

B173HW02 V1 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

| Items | Unit | Specifications | | | |
|--|----------------------|--|-------|-------|-------|
| Screen Diagonal | [mm] | 17.3W"(17.25) | | | |
| Active Area | [mm] | 381.888 X 214.812 | | | |
| Pixels H x V | | 1920x3(RGB) x1080 | | | |
| Pixel Pitch | [mm] | 0.1989X0.1989 | | | |
| Pixel Format | | R.G.B. Vertical Stripe | | | |
| Display Mode | | Normally White | | | |
| White Luminance (ILED=20mA) (Note: ILED is LED current) | [cd/m ²] | 300 typ. (5 points average) 255 min. (5 points average) | | | |
| Luminance Uniformity | | 1.25 max. (5 points) / 1.35 max. (13 points) | | | |
| Contrast Ratio | | 400 typ | | | |
| Response Time | [ms] | 8 typ / 16 Max | | | |
| Nominal Input Voltage VDD | [Volt] | +3.3 typ. | | | |
| Power Consumption | [Watt] | 9.0 max. (Include Logic and Blu power) | | | |
| Weight | [Grams] | 590 max. | | | |
| Physical Size Include bracket | [mm] | | Min. | Typ. | Max. |
| | | Length | 397.6 | 398.1 | 398.6 |
| | | Width | 232.3 | 232.8 | 233.3 |
| | | Thickness | --- | --- | 6.0 |
| Electrical Interface | | 2 channel LVDS | | | |
| Glass Thickness | [mm] | 0.5 | | | |
| Surface Treatment | | Anti-Glare | | | |
| Support Color | | 262K colors (RGB 6-bit) | | | |
| Temperature Range | | | | | |
| Operating | [°C] | 0 to +50 | | | |
| Storage (Non-Operating) | [°C] | -20 to +60 | | | |
| RoHS Compliance | | RoHS Compliance | | | |



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2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

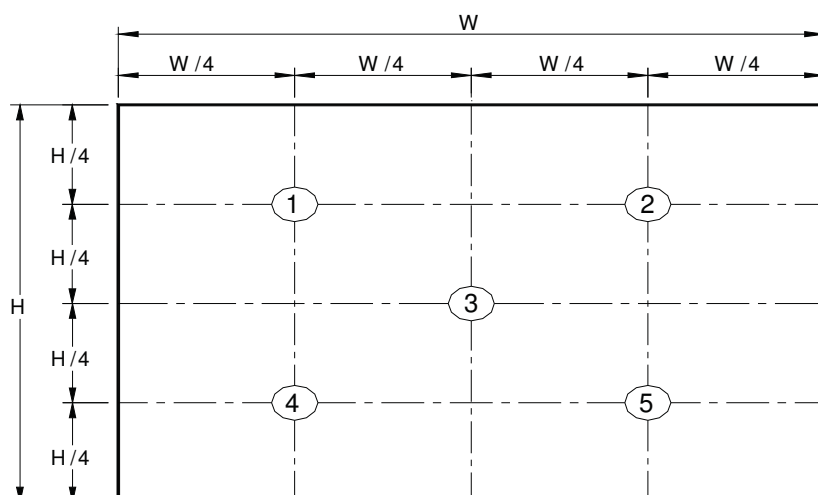
| Item | | Symbol | Conditions | Min. | Typ. | Max. | Unit | Note | | | |
|--|-------|-----------------|--------------------------------------|-------|-------|-------|-------------------|----------|----|-----|--|
| White Luminance ILED=20mA | | | 5 points average | 255 | 300 | --- | cd/m ² | 1, 4, 5. | | | |
| Viewing Angle | | θ_R | Horizontal (Right) CR = 10 (Left) | 60 | 70 | --- | degree | 4, 9 | | | |
| | | θ_L | | 60 | 70 | --- | | | | | |
| | | ψ_H | Vertical (Upper) CR = 10 (Lower) | 45 | 60 | --- | | | | | |
| | | ψ_L | | 50 | 60 | --- | | | | | |
| Luminance Uniformity | | δ_{5P} | 5 Points | --- | --- | 1.25 | | 1, 3, 4 | | | |
| Luminance Uniformity | | δ_{13P} | 13 Points | --- | --- | 1.42 | | 2, 3, 4 | | | |
| Contrast Ratio | | CR | | 300 | 400 | --- | | 4, 6 | | | |
| Cross talk | | % | | --- | --- | 4 | | 4, 7 | | | |
| Response Time | | T _{RT} | Rising + Falling | --- | 8 | 16 | msec | 4, 8 | | | |
| Color / Chromaticity Coordinates | Red | R _x | CIE 1931 | TBD | TBD | TBD | --- | 4 | | | |
| | | R _y | | TBD | TBD | TBD | | | | | |
| | Green | G _x | | TBD | TBD | TBD | | | | | |
| | | G _y | | TBD | TBD | TBD | | | | | |
| | Blue | B _x | | TBD | TBD | TBD | | | | | |
| | | B _y | | TBD | TBD | TBD | | | | | |
| | White | W _x | | 0.283 | 0.313 | 0.342 | | | | | |
| | | W _y | | 0.299 | 0.329 | 0.359 | | | | | |
| | NTSC | | | % | | --- | | | 72 | --- | |



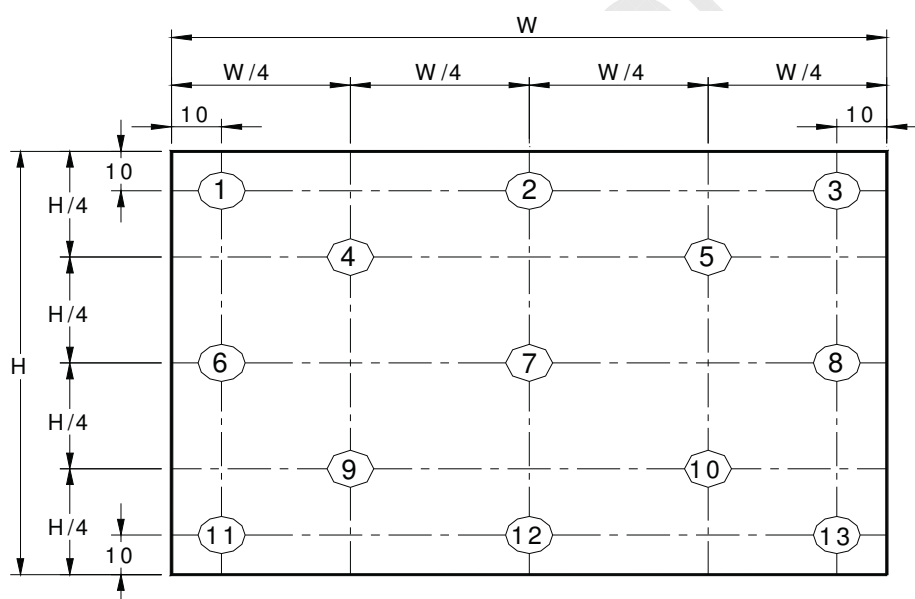
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Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

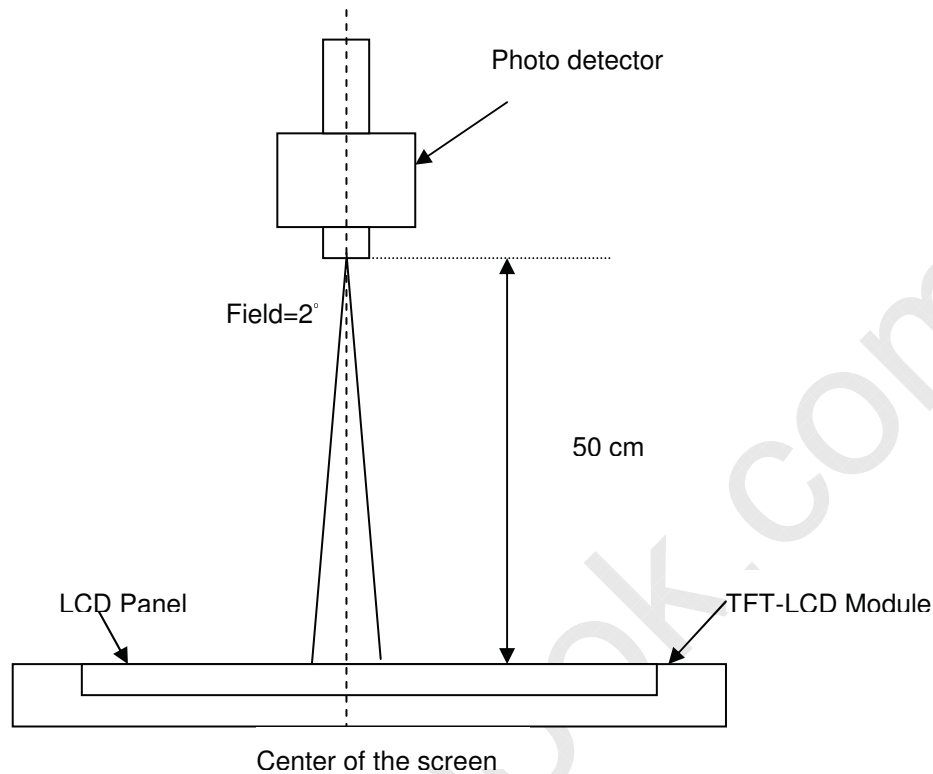
The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight



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for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5 : Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points , $Y_L = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$

$L(x)$ is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

Note 7 : Definition of Cross Talk (CT)

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

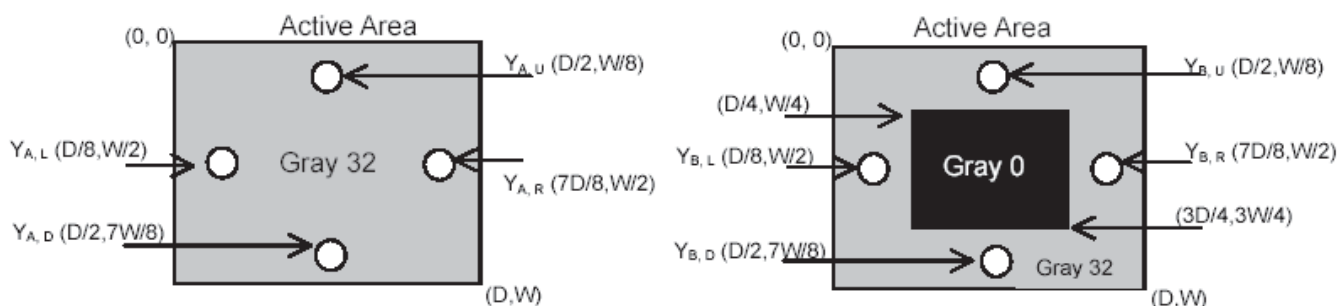
Y_A = Luminance of measured location without gray level 0 pattern (cd/m²)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m²)



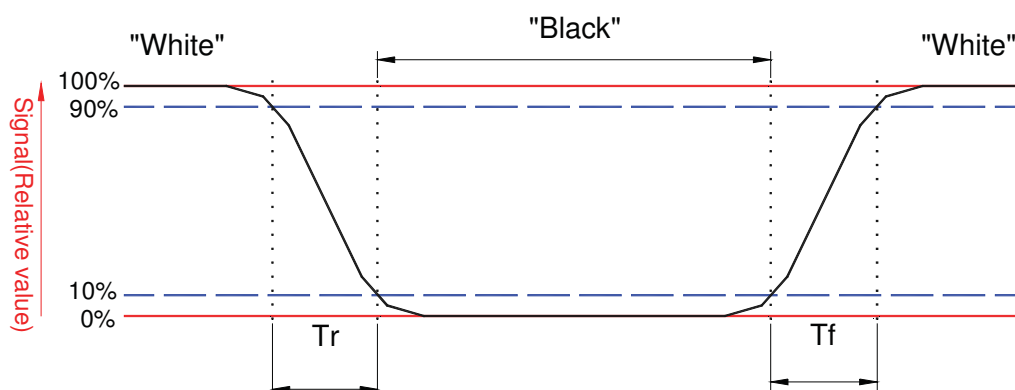
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Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



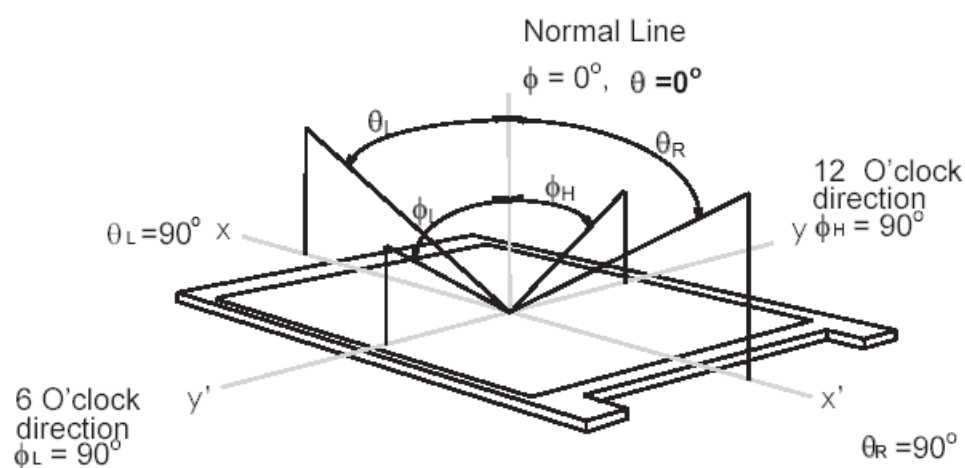


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Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10 , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (ϕ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



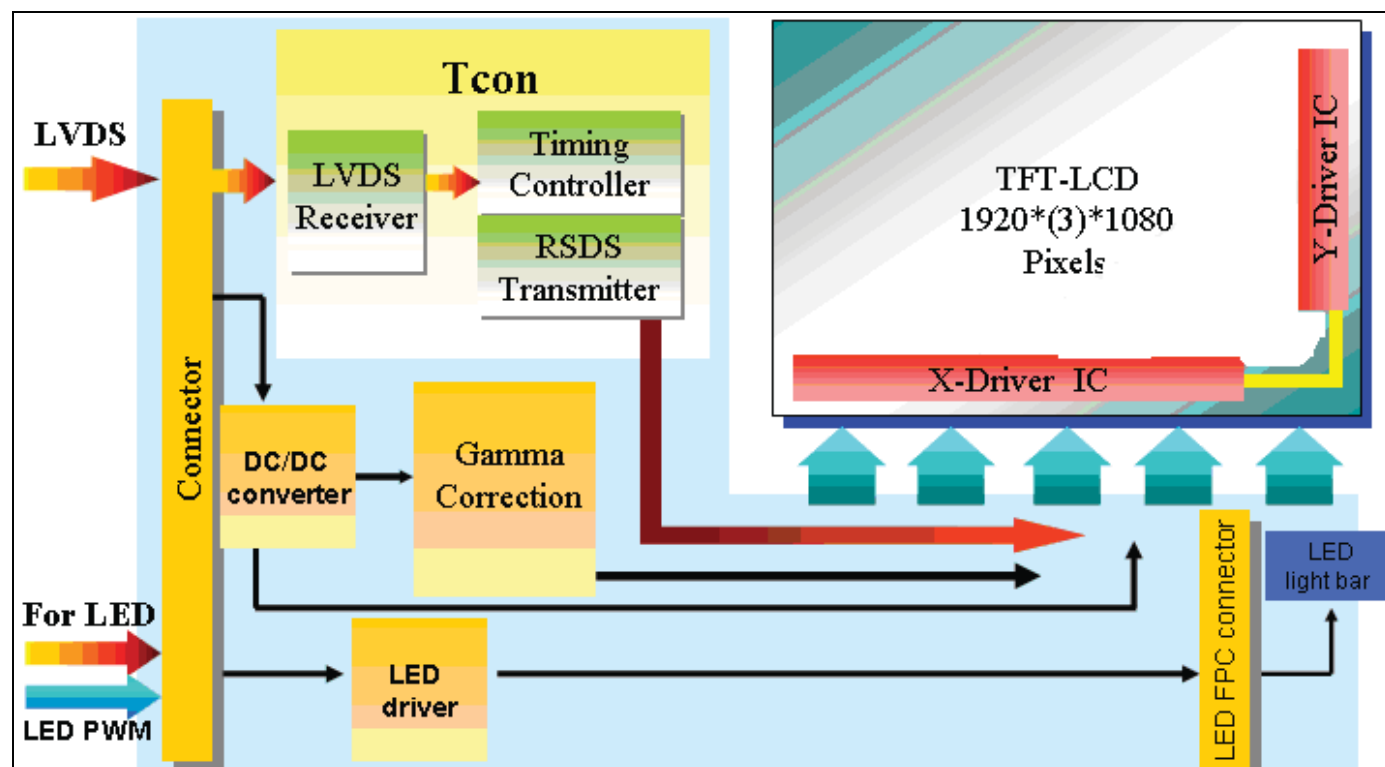


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3. Functional Block Diagram

The following diagram shows the functional block of the 17.3 inches wide Color TFT/LCD 40 Pin two channel Module





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4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

| Item | Symbol | Min | Max | Unit | Conditions |
|-------------------------|--------|------|------|--------|------------|
| Logic/LCD Drive Voltage | Vin | -0.3 | +4.0 | [Volt] | Note 1,2 |

4.2 Absolute Ratings of Environment

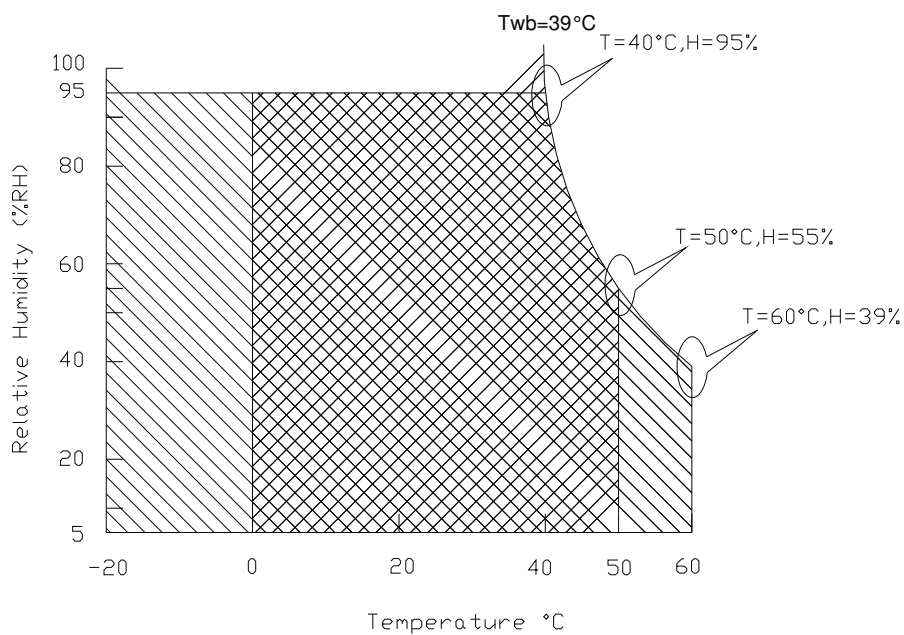
| Item | Symbol | Min | Max | Unit | Conditions |
|-----------------------|--------|-----|-----|-------|------------|
| Operating Temperature | TOP | 0 | +50 | [°C] | Note 4 |
| Operation Humidity | HOP | 5 | 95 | [%RH] | Note 4 |
| Storage Temperature | TST | -20 | +60 | [°C] | Note 4 |
| Storage Humidity | HST | 5 | 95 | [%RH] | Note 4 |

Note 1: At Ta (25°C)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range

Storage Range +



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5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

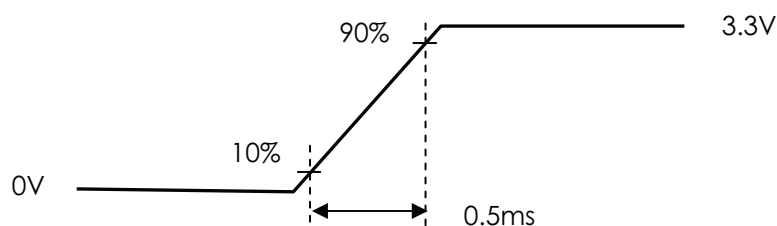
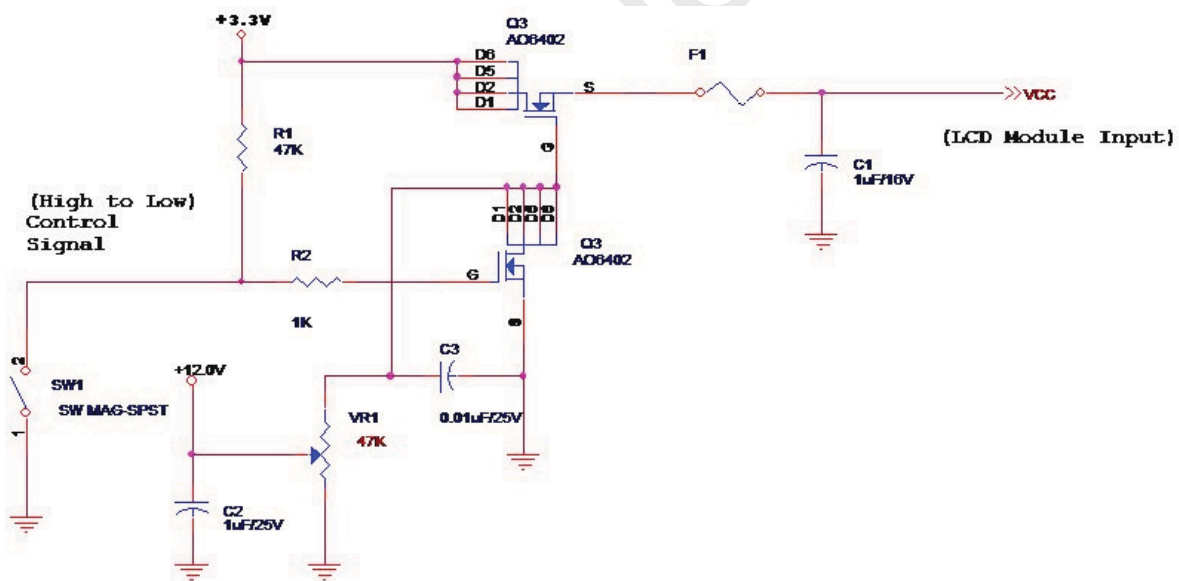
Input power specifications are as follows;

The power specification are measured under 25°C and frame frequency under 60Hz

| Symble | Parameter | Min | Typ | Max | Units | Note |
|--------|--|-----|-----|------|-------------|--------|
| VDD | Logic/LCD Drive Voltage | 3.0 | 3.3 | 3.6 | [Volt] | |
| PDD | VDD Power | - | - | 2 | [Watt] | Note 1 |
| IDD | IDD Current | - | 350 | 600 | [mA] | Note 1 |
| IRush | Inrush Current | - | - | 2000 | [mA] | Note 2 |
| VDDrp | Allowable Logic/LCD Drive Ripple Voltage | - | - | 100 | [mV] p-p | |

Note 1 : Maximum Measurement Condition : Black Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{black}$)

Note 2 : Measure Condition



Vin rising time



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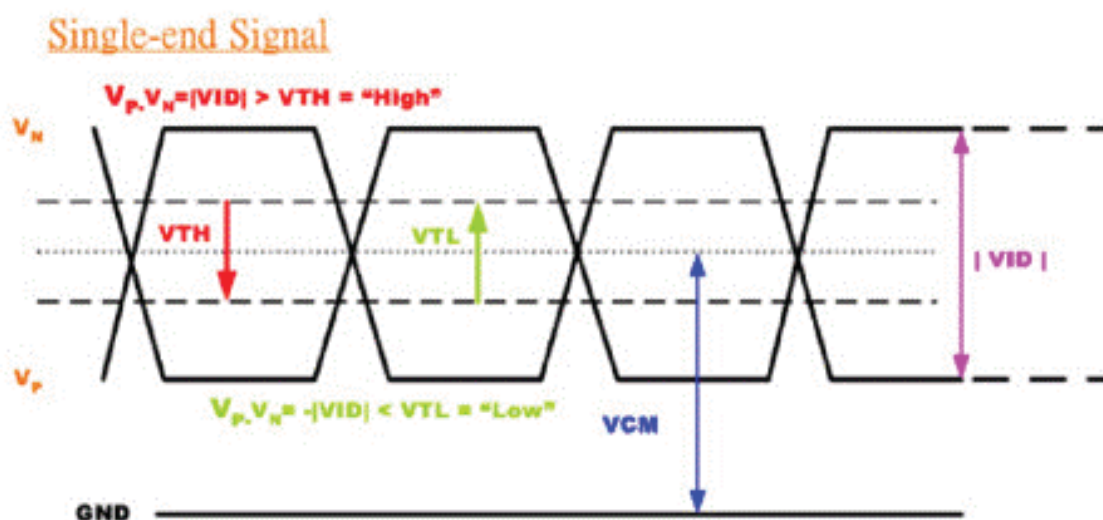
5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

| Parameter | Condition | Min | Max | Unit |
|-----------|--|-------|-------|------|
| V_{th} | Differential Input High Threshold ($V_{cm}=+1.2V$) | --- | 100 | [mV] |
| V_{tl} | Differential Input Low Threshold ($V_{cm}=+1.2V$) | -100 | --- | [mV] |
| V_{ID} | Differential Input Voltage | 100 | 600 | [mV] |
| V_{cm} | Differential Input Common Mode Voltage | 1.125 | 1.375 | [V] |

Note: LVDS Signal Waveform





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5.2 Backlight Unit

5.2.1 LED characteristics

| Parameter | Symbol | Min | Typ | Max | Units | Condition |
|-----------------------------|--------|--------|-----|-----|--------|------------------------------|
| Backlight Power Consumption | PLED | - | - | 7 | [Watt] | (Ta=25℃), Note 1. Vin=12V |
| LED Life-Time | N/A | 10,000 | - | - | Hour | (Ta=25℃), Note 2 If=20 mA |

Note 1: Calculator value for reference $P_{LED} = V_F$ (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

| Parameter | Symbol | Min | Typ | Max | Units | Remark |
|-----------------------------|---------|-----|------|------|--------|---|
| LED Power Supply | VLED | 7.0 | 12.0 | 21.0 | [Volt] | Define as Connector Interface (Ta=25℃) |
| LED Enable Input High Level | VLED_EN | 2.5 | - | 5.5 | [Volt] | |
| LED Enable Input Low Level | | - | - | 0.8 | [Volt] | |
| PWM Logic Input High Level | VPWM_EN | 2.5 | - | 5.5 | [Volt] | |
| PWM Logic Input Low Level | | - | - | 0.8 | [Volt] | |
| PWM Input Frequency | FPWM | 100 | 1K | 20K | Hz | |
| PWM Duty Ratio | Duty | 5 | -- | 100 | % | |



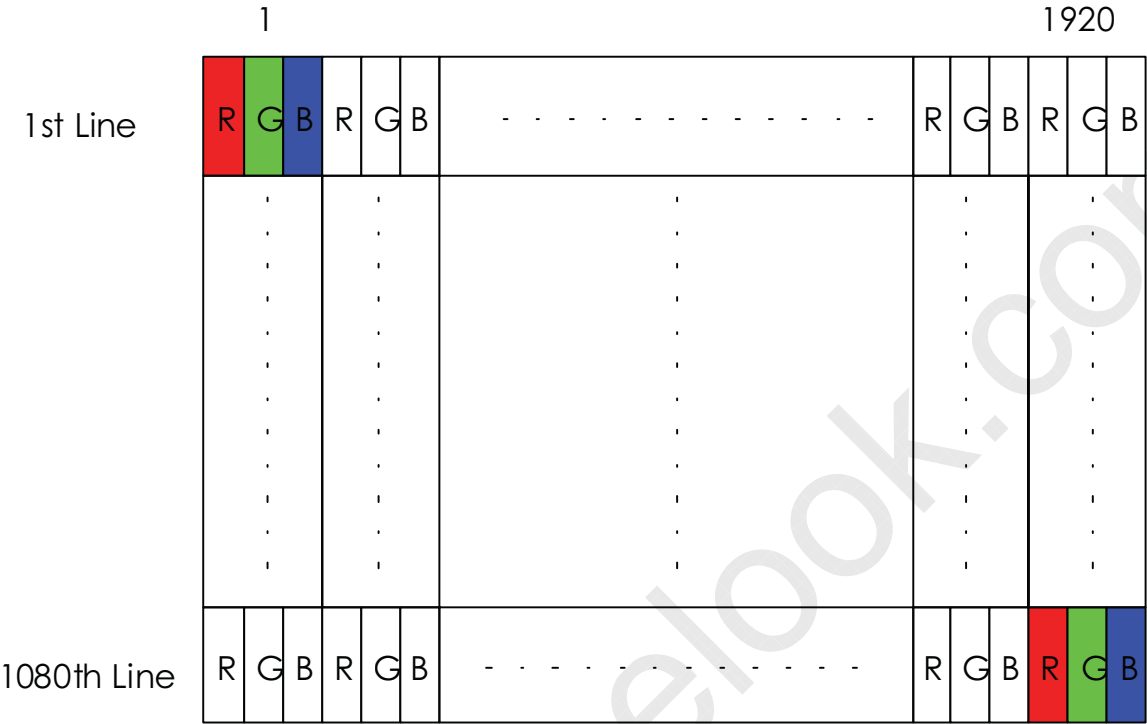
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6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.

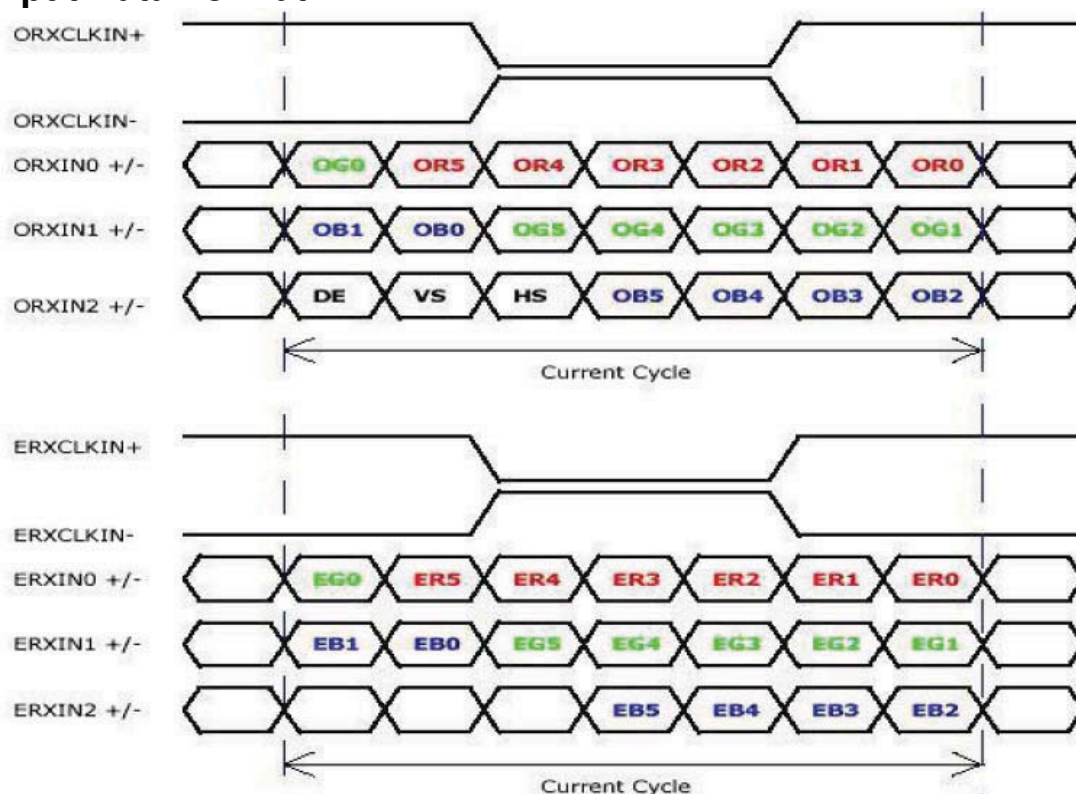




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6.2 The Input Data Format



| Signal Name | Description | |
|----------------------------------|--|---|
| R5 R4 R3 R2 R1 R0 | Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data | Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data. |
| G5 G4 G3 G2 G1 G0 | Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data | Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data. |
| B5 B4 B3 B2 B1 B0 | Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data | Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data. |
| RxCLKIN | Data Clock | The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high. |
| DE | Display Timing | This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed. |
| VS | Vertical Sync | The signal is synchronized to RxCLKIN. |
| HS | Horizontal Sync | The signal is synchronized to RxCLKIN. |

Note: Output signals from any system shall be low or High-impedance state when VDD is off.



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6.3 Integration Interface Requirement

6.3.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

| Connector Name / Designation | For Signal Connector |
|------------------------------|------------------------------|
| Manufacturer | JAE or Compatible |
| Type / Part Number | JAE HD1S040HA1 or Compatible |
| Mating Housing/Part Number | JAE HD1S040HA1 or Compatible |

6.3.2 Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

| PIN# | Signal Name | Description |
|------|-------------|---|
| 1 | NC | No Connection |
| 2 | VDD | Power Supply +3.3V |
| 3 | VDD | Power Supply +3.3V |
| 4 | VEDID | EDID +3.3V Power |
| 5 | NC | No Connect (Reserve for M1 aging) |
| 6 | CLKEDID | EDID Clock Input |
| 7 | DATAEDID | EDID Data Input |
| 8 | RxOIN0- | -LVDS Differential Data INPUT(Odd R0-R5,G0) |
| 9 | RxOIN0+ | +LVDS Differential Data INPUT(Odd R0-R5,G0) |
| 10 | VSS | Ground |
| 11 | RxOIN1- | -LVDS Differential Data INPUT(Odd G1-G5,B0-B1) |
| 12 | RxOIN1+ | +LVDS Differential Data INPUT(Odd G1-G5,B0-B1) |
| 13 | VSS | Ground |
| 14 | RxOIN2- | -LVDS Differential Data INPUT(Odd B2-B5,HS,VS,DE) |
| 15 | RxOIN2+ | +LVDS Differential Data INPUT(Odd B2-B5,HS,VS,DE) |
| 16 | VSS | Ground |
| 17 | RxOCKIN- | -LVDS Odd Differential Clock INPUT |
| 18 | RxOCKIN+ | +LVDS Odd Differential Clock INPUT |
| 19 | VSS | Ground |
| 20 | RxEIN0- | -LVDS Differential Data INPUT(Even R0-R5,G0) |
| 21 | RxEIN0+ | +LVDS Differential Data INPUT(Even R0-R5,G0) |
| 22 | VSS | Ground |



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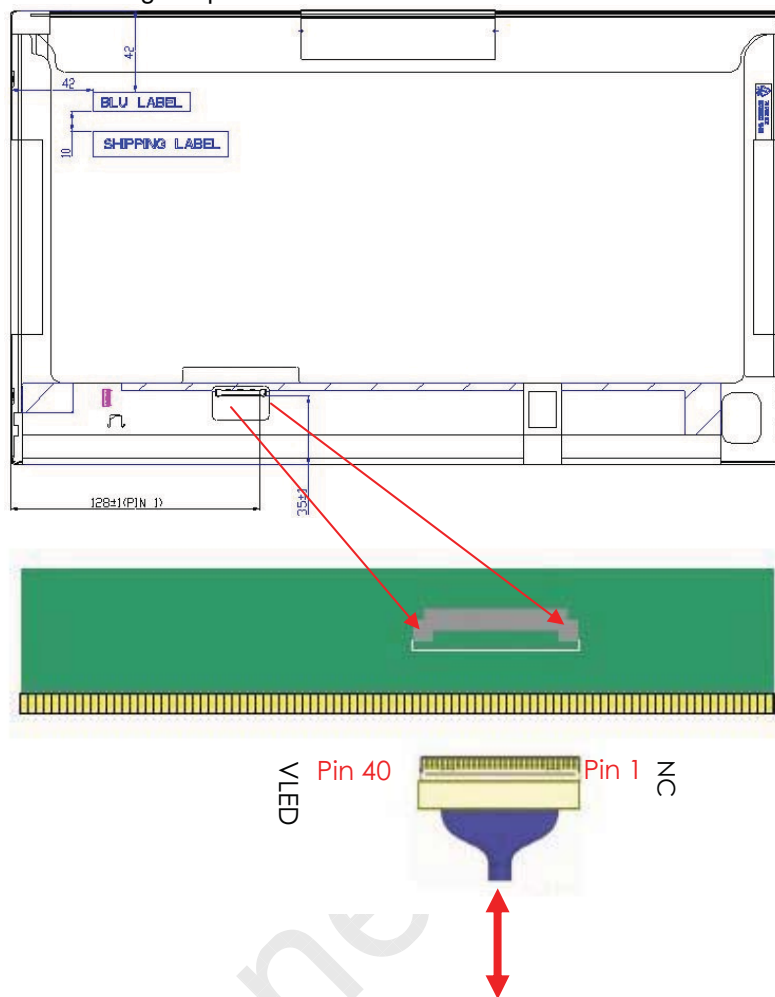
| | | |
|----|----------|--|
| 23 | RxEIN1- | -LVDS Differential Data INPUT(Even G1-G5,B0-B1) |
| 24 | RxEIN1+ | +LVDS Differential Data INPUT(Even G1-G5,B0-B1) |
| 25 | VSS | Ground |
| 26 | RxEIN2- | -LVDS Differential Data INPUT(Even B2-B5,HS,VS,DE) |
| 27 | RxEIN2+ | +LVDS Differential Data INPUT(Even B2-B5,HS,VS,DE) |
| 28 | VSS | Ground |
| 29 | RxECKIN- | -LVDS Even Differential Clock INPUT |
| 30 | RxECKIN+ | +LVDS Even Differential Clock INPUT |
| 31 | VLED_GND | LED Ground |
| 32 | VLED_GND | LED Ground |
| 33 | VLED_GND | LED Ground |
| 34 | NC | No Connection |
| 35 | S_PWMIN | System PWM Logic Input level |
| 36 | LED_EN | LED enable input level |
| 37 | NC | No Connection |
| 38 | VLED | LED Power Supply |
| 39 | VLED | LED Power Supply |
| 40 | VLED | LED Power Supply |



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Note1: Input signals shall be low or High-impedance state when VDD is off.



Note1: Input signals shall be low or High-impedance state when VDD is off.



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6.4 Interface Timing

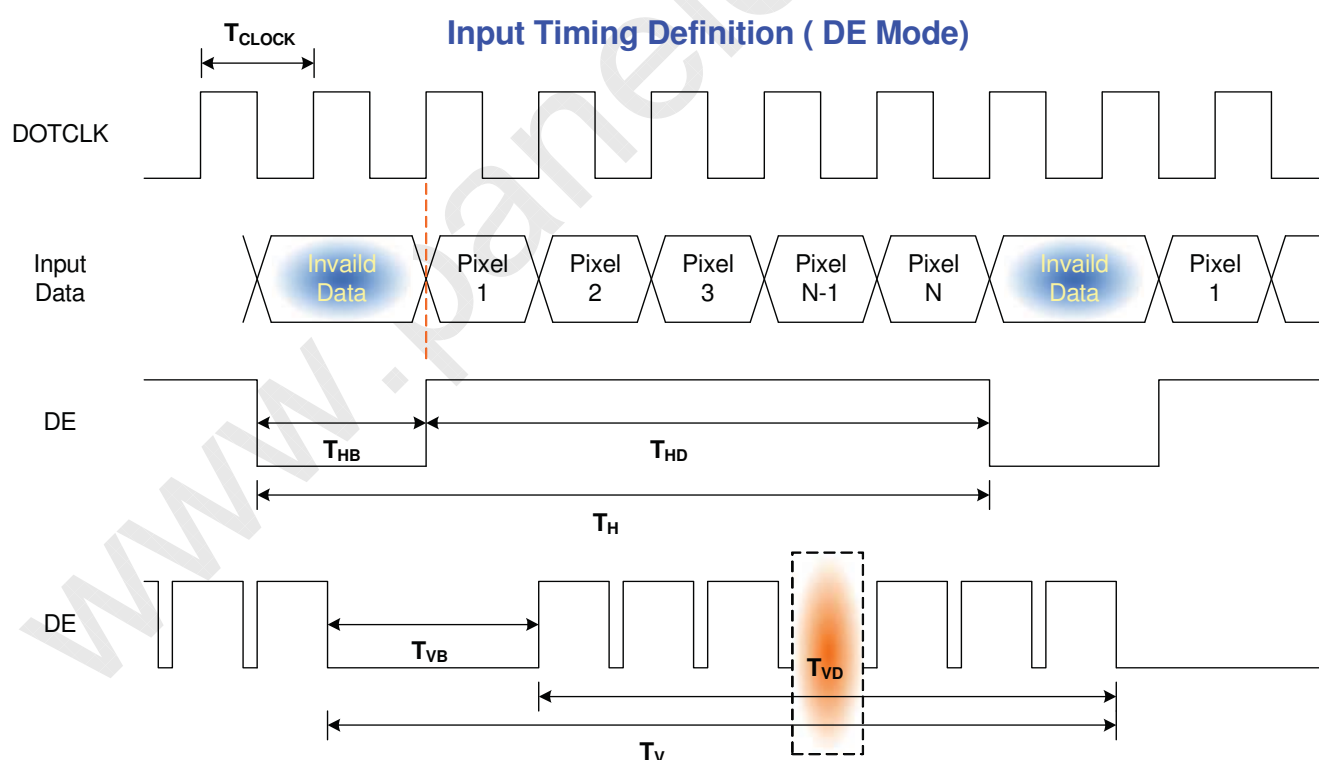
6.4.1 Timing Characteristics

Basically, interface timings should match the 1920X1080 / 60Hz manufacturing guide line timing.

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|-----------------------|----------|-----------------------|------|------|------|--------------------|
| Frame Rate | | - | 50 | 60 | - | Hz |
| Clock frequency | | 1/ T _{Clock} | 50 | 74.9 | 85 | MHz |
| Vertical Section | Period | T _V | 1088 | 1130 | 1680 | T _{Line} |
| | Active | T _{VD} | 1080 | | | |
| | Blanking | T _{VB} | 8 | 50 | - | |
| Horizontal Section | Period | T _H | 990 | 1050 | - | T _{Clock} |
| | Active | T _{HD} | 960 | | | |
| | Blanking | T _{HB} | 30 | 90 | - | |

Note : DE mode only

6.4.2 Timing diagram



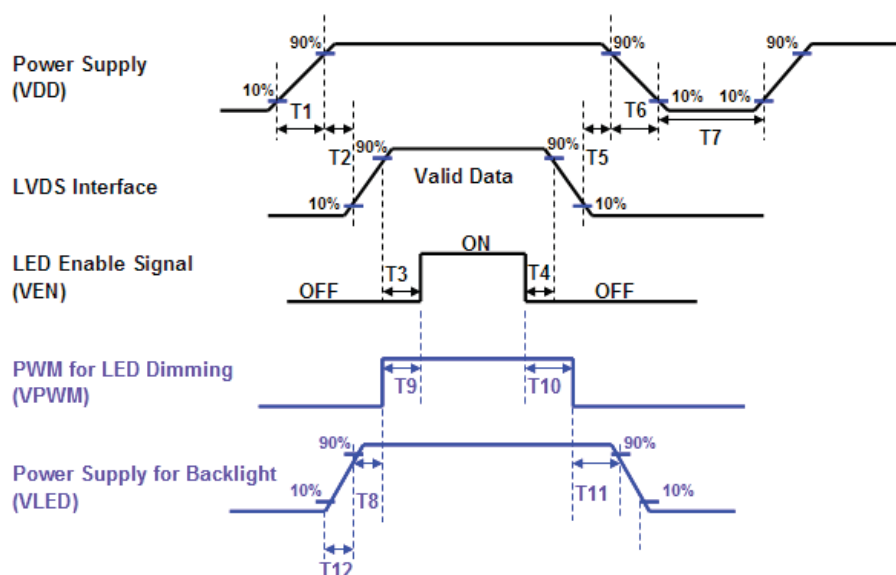


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6.5 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off



Wiat for check with system

| Power Sequence Timing | | |
|-----------------------|------------------|------|
| Parameter | Value(Units: ms) | |
| | Min. | Max. |
| T1 | 0.5 | 10 |
| T2 | 0 | 50 |
| T3 | 200 | - |
| T4 | 200 | - |
| T5 | 0 | 50 |
| T6 | 0 | 10 |
| T7 | 500 | - |
| T8 | 10 | - |
| T9 | 10 | 180 |
| T10 | 10 | 180 |
| T11 | 10 | - |
| T12 | 0.5 | 10 |



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7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

| Items | Required Condition | Note |
|----------------------------|---|--------|
| Temperature Humidity Bias | Ta= 40℃ , 90%RH, 300h | |
| High Temperature Operation | Ta= 50℃ , Dry, 300h | |
| Low Temperature Operation | Ta= 0℃ , 300h | |
| High Temperature Storage | Ta= 60℃ , 35%RH, 300h | |
| Low Temperature Storage | Ta= -20℃ , 50%RH, 250h | |
| Thermal Shock Test | Ta=-20℃ to 60℃ , Duration at 30 min, 100 cycles | |
| ESD | Contact : ±8 KV Air : ±15 KV | Note 1 |

Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost
Self-recoverable. No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

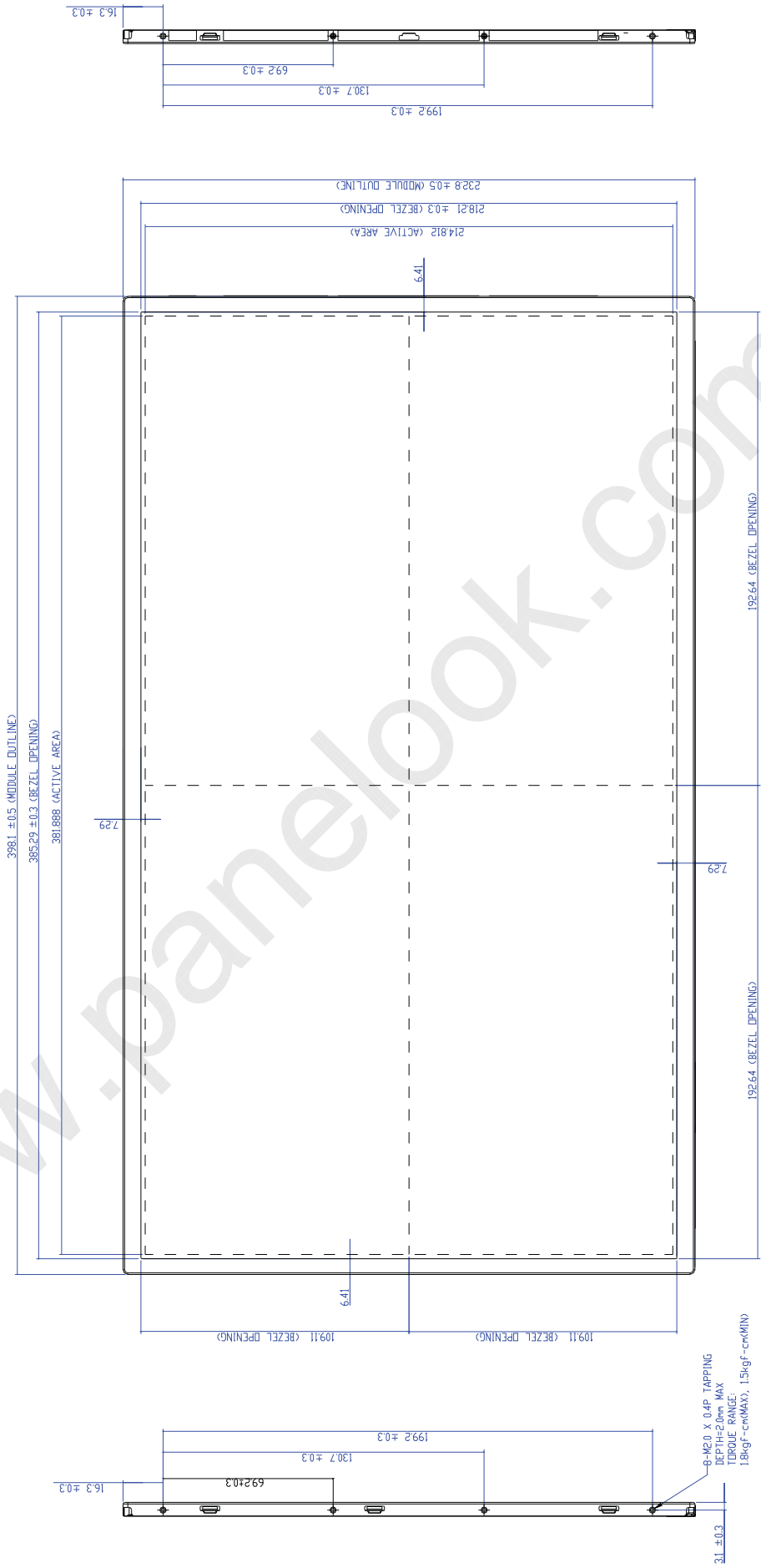


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8. Mechanical Characteristics

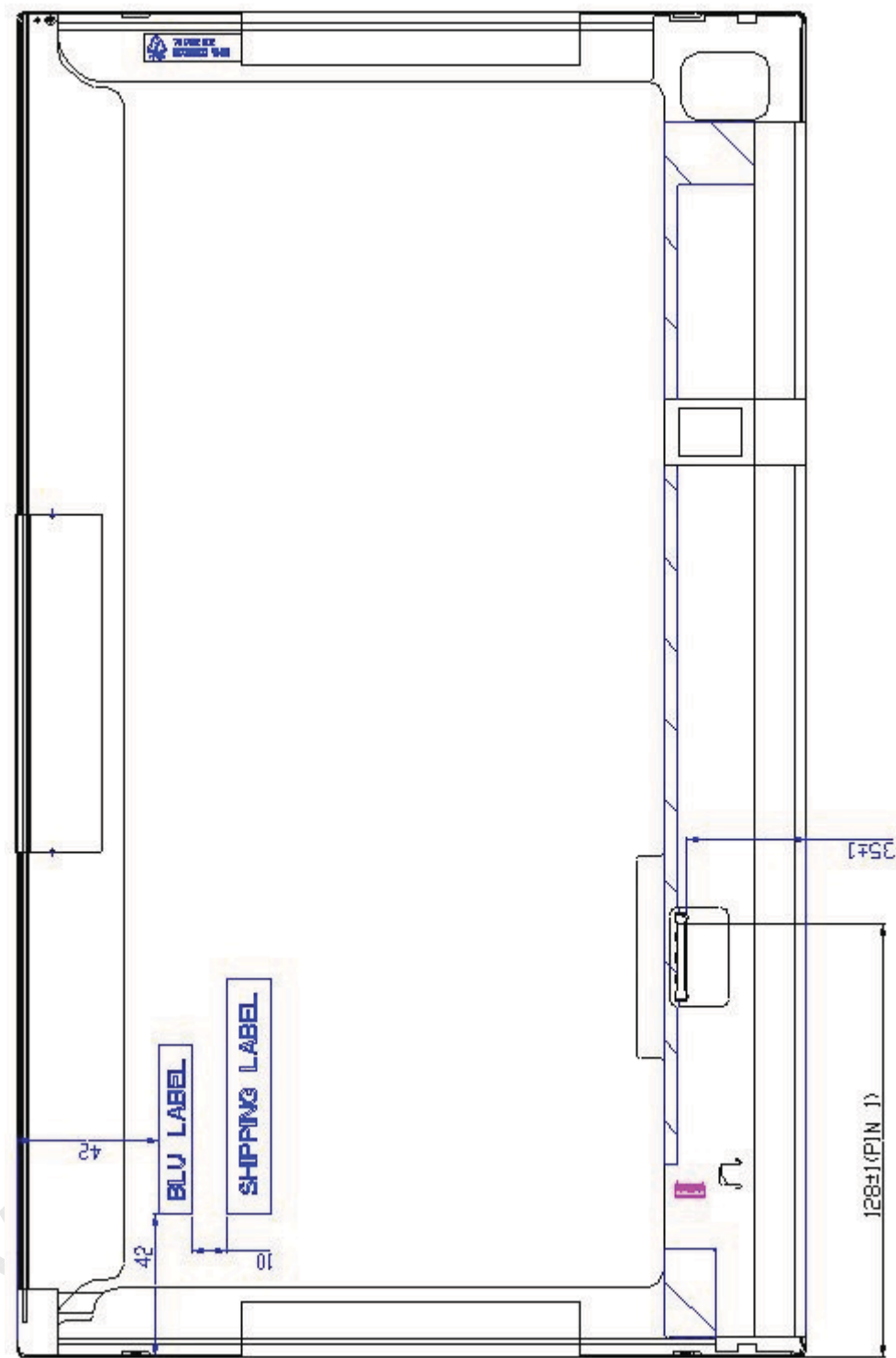
8.1 LCM Outline Dimension





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Note: Prevention IC damage, IC positions not allowed any overlap over these areas.



Product Specification

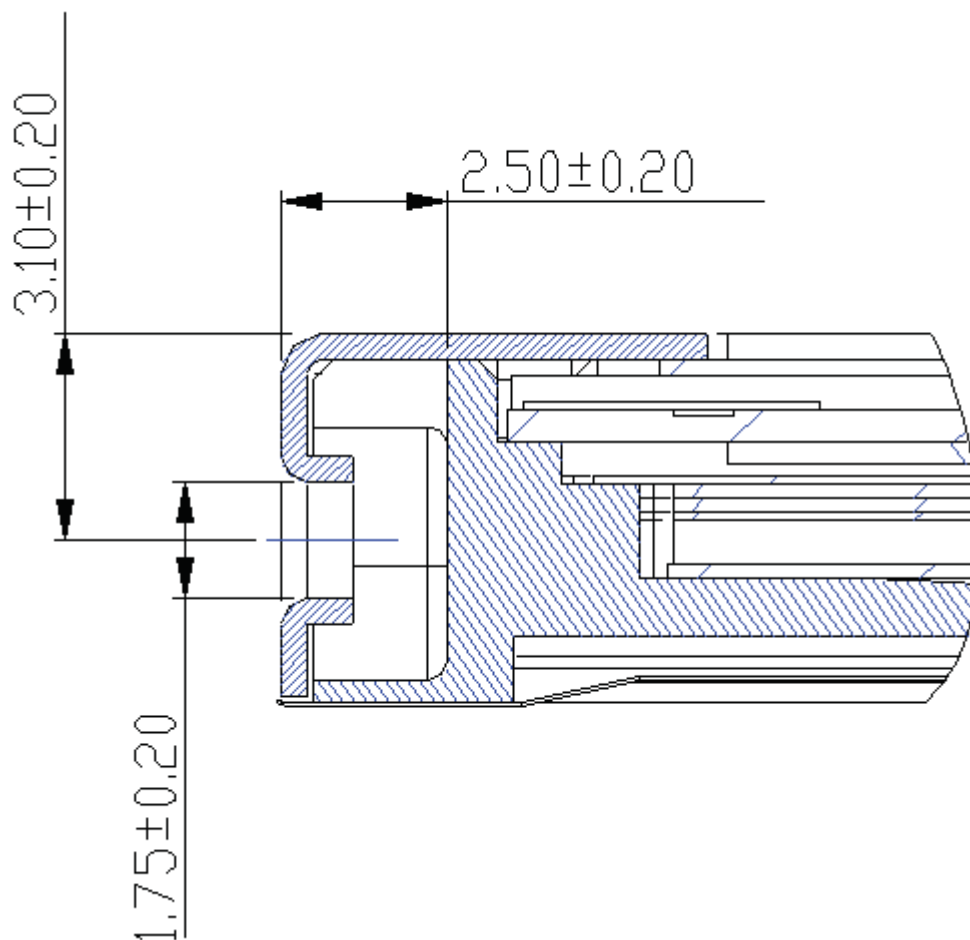
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8.2 Screw Hole Depth and Center Position

Maximum Screw penetration from side surface is 2.3 mm

The center of screw hole center location is $3.1 \pm 0.2\text{mm}$ from front surface

Screw Torque: Maximum 2.5 kgf-cm







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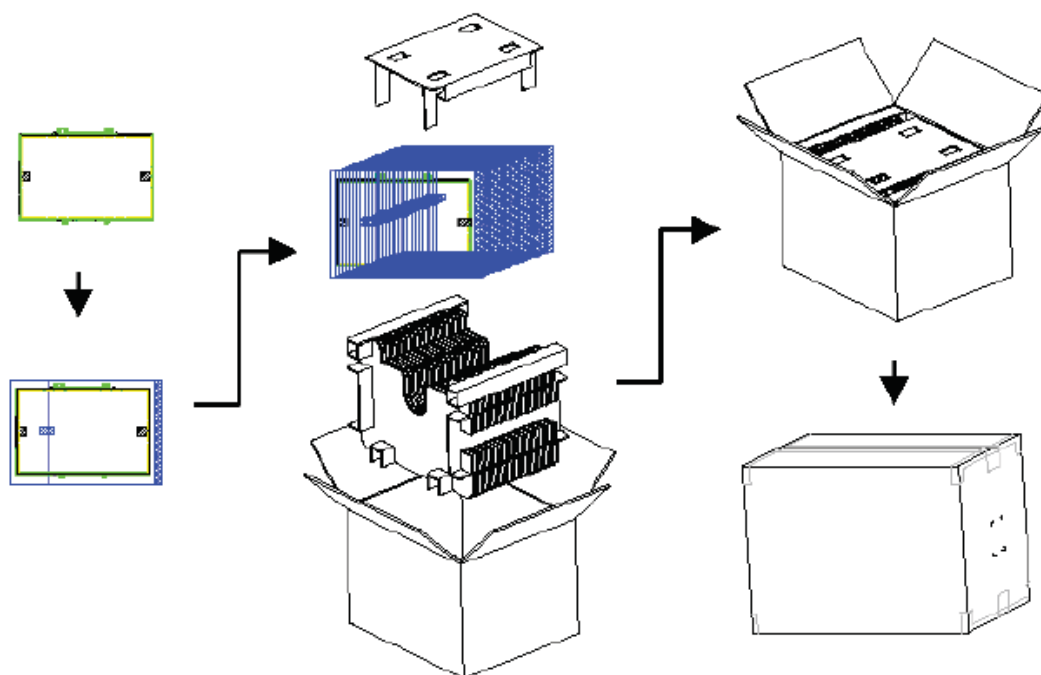
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9. Shipping and Package

9.1 Shipping Label Format

| | | | |
|--|---|---|---|
|  XXXXXXXXXXXX-XXXXXX | Manufactured MM/WW Model No: B173HW02 V1 AU Optronics MADE IN CHINA (S01) H/W: 0A F/W:1 | c  US E204356 |    |
|--|---|---|---|

9.2 Carton Package

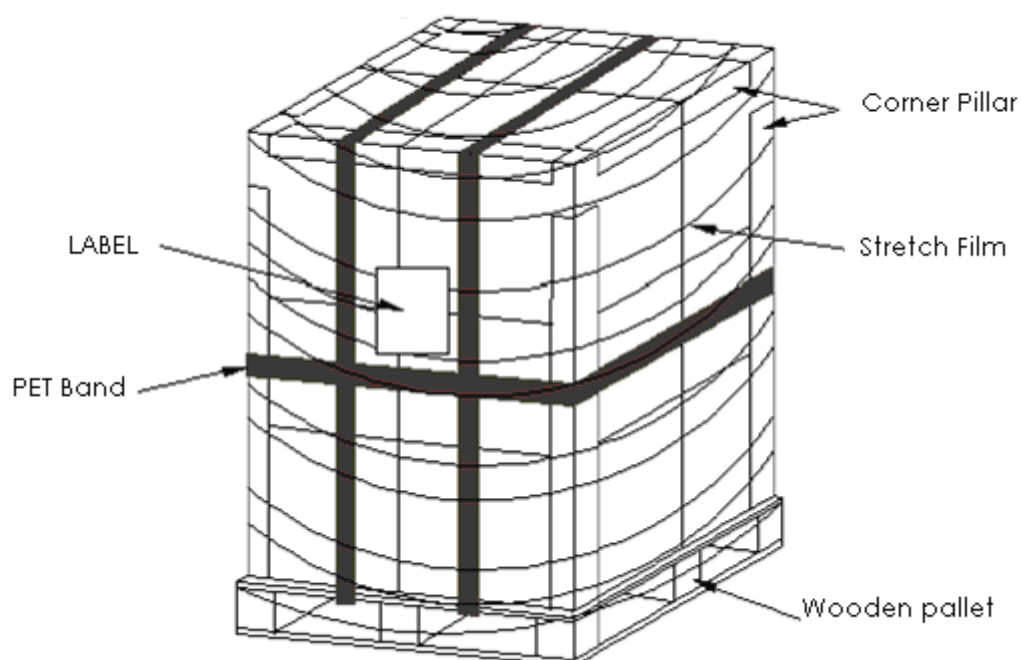




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9.3 Shipping Package of Palletizing Sequence





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10. Appendix: EDID Description

| | Byte (hex) | Field Name and Comments | Value (hex) | Value (binary) | Value (DEC) |
|----------------------------------|---------------|--|----------------|-------------------|----------------|
| Header | 0 | Header | TBD | TBD | TBD |
| | 1 | Header | TBD | TBD | TBD |
| | 2 | Header | TBD | TBD | TBD |
| | 3 | Header | TBD | TBD | TBD |
| | 4 | Header | TBD | TBD | TBD |
| | 5 | Header | TBD | TBD | TBD |
| | 6 | Header | TBD | TBD | TBD |
| | 7 | Header | TBD | TBD | TBD |
| Vendor / Product EDID Version | 8 | EISA manufacture code = 3 Character ID | TBD | TBD | TBD |
| | 9 | EISA manufacture code (Compressed ASCII) | TBD | TBD | TBD |
| | 0A | Panel Supplier Reserved – Product Code | TBD | TBD | TBD |
| | 0B | Panel Supplier Reserved – Product Code | TBD | TBD | TBD |
| | 0C | LCD module Serial No - Preferred but Optional (“0” if not used) | TBD | TBD | TBD |
| | 0D | LCD module Serial No - Preferred but Optional (“0” if not used) | TBD | TBD | TBD |
| | 0E | LCD module Serial No - Preferred but Optional (“0” if not used) | TBD | TBD | TBD |
| | 0F | LCD module Serial No - Preferred but Optional (“0” if not used) | TBD | TBD | TBD |
| | 10 | Week of manufacture | TBD | TBD | TBD |
| | 11 | Year of manufacture | TBD | TBD | TBD |
| | 12 | EDID structure version # = 1 | TBD | TBD | TBD |
| | 13 | EDID revision # = 4 | TBD | TBD | TBD |
| Display Parameters | 14 | Video I/P definition = Digital I/P (90 (6-bit) or A0 (8-Bit)) | TBD | TBD | TBD |
| | 15 | Max H image size = ?? cm(Rounded to cm) | TBD | TBD | TBD |
| | 16 | Max V image size = ?? cm(Rounded to cm) | TBD | TBD | TBD |
| | 17 | Display gamma = (gamma ×100)-100 = Example: (2.2×100) – 100 = 120 | TBD | TBD | TBD |
| | 18 | Feature support | TBD | TBD | TBD |
| Panel Color Coordinates | 19 | Red/Green Low bit (RxRy/GxGy) | TBD | TBD | TBD |
| | 1A | Blue/White Low bit (BxBy/WxWy) | TBD | TBD | TBD |
| | 1B | Red X Rx = 0.??? | TBD | TBD | TBD |
| | 1C | Red Y Ry = 0.??? | TBD | TBD | TBD |
| | 1D | Green X Rx = 0.??? | TBD | TBD | TBD |
| | 1E | Green Y Ry = 0.??? | TBD | TBD | TBD |
| | 1F | Blue X Rx = 0.??? | TBD | TBD | TBD |
| | 20 | Blue Y Ry = 0.??? | TBD | TBD | TBD |
| | 21 | White X Rx = 0.??? | TBD | TBD | TBD |
| | 22 | White Y Ry = 0.??? | TBD | TBD | TBD |



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| | | | | | |
|----------------------|----|---|-----|-----|-----|
| Established Timings | 23 | Established timings 1 (00h if not used) | TBD | TBD | TBD |
| | 24 | Established timings 2 (00h if not used) | TBD | TBD | TBD |
| | 25 | Manufacturer's timings (00h if not used) | TBD | TBD | TBD |
| Standard Timing ID | 26 | Standard timing ID1 (01h if not used) | TBD | TBD | TBD |
| | 27 | Standard timing ID1 (01h if not used) | TBD | TBD | TBD |
| | 28 | Standard timing ID2 (01h if not used) | TBD | TBD | TBD |
| | 29 | Standard timing ID2 (01h if not used) | TBD | TBD | TBD |
| | 2A | Standard timing ID3 (01h if not used) | TBD | TBD | TBD |
| | 2B | Standard timing ID3 (01h if not used) | TBD | TBD | TBD |
| | 2C | Standard timing ID4 (01h if not used) | TBD | TBD | TBD |
| | 2D | Standard timing ID4 (01h if not used) | TBD | TBD | TBD |
| | 2E | Standard timing ID5 (01h if not used) | TBD | TBD | TBD |
| | 2F | Standard timing ID5 (01h if not used) | TBD | TBD | TBD |
| | 30 | Standard timing ID6 (01h if not used) | TBD | TBD | TBD |
| | 31 | Standard timing ID6 (01h if not used) | TBD | TBD | TBD |
| | 32 | Standard timing ID7 (01h if not used) | TBD | TBD | TBD |
| | 33 | Standard timing ID7 (01h if not used) | TBD | TBD | TBD |
| | 34 | Standard timing ID8 (01h if not used) | TBD | TBD | TBD |
| | 35 | Standard timing ID8 (01h if not used) | TBD | TBD | TBD |
| Timing Descriptor #1 | 36 | Pixel Clock/10,000 (LSB) | TBD | TBD | TBD |
| | 37 | Pixel Clock/10,000 (MSB) | TBD | TBD | TBD |
| | 38 | Horizontal Active = ??? pixels (lower 8 bits) | TBD | TBD | TBD |
| | 39 | Horizontal Blanking (Thbp) = 320 pixels (lower 8 bits) | TBD | TBD | TBD |
| | 3A | Horizontal Active/Horizontal blanking (Thbp) (upper 4:4 bits) | TBD | TBD | TBD |
| | 3B | Vertical Active = ??? lines | TBD | TBD | TBD |
| | 3C | Vertical Blanking (Tvbp) = ?? lines (DE Blanking typ. for DE only panels) | TBD | TBD | TBD |
| | 3D | Vertical Active : Vertical Blanking (Tvbp) (upper 4:4 bits) | TBD | TBD | TBD |
| | 3E | Horizontal Sync, Offset (Thfp) = ?? pixels | TBD | TBD | TBD |
| | 3F | Horizontal Sync, Pulse Width = ??? pixels | TBD | TBD | TBD |
| | 40 | Vertical Sync, Offset (Tvfp) = ? lines Sync Width = ? lines | TBD | TBD | TBD |
| | 41 | Horizontal Vertical Sync Offset/Width upper 2 bits | TBD | TBD | TBD |
| | 42 | Horizontal Image Size = ??? mm | TBD | TBD | TBD |
| | 43 | Vertical image Size = ??? mm | TBD | TBD | TBD |
| | 44 | Horizontal Image Size / Vertical image size | TBD | TBD | TBD |
| | 45 | Horizontal Border = 0 (Zero for Notebook LCD) | TBD | TBD | TBD |
| | 46 | Vertical Border = 0 (Zero for Notebook LCD) | TBD | TBD | TBD |



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| | | | | | |
|---|----|--|-----|-----|-----|
| | 47 | Bit[7] 0 : Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] : The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see VESA EDID Spec 1.3 Bit[0] : See VESA EDID Spec 1.3 ==> fix=1A | TBD | TBD | TBD |
| Timing Descriptor #2 (=Timing Descriptor #1) | 48 | Pixel Clock/10,000 (LSB) | TBD | TBD | TBD |
| | 49 | Pixel Clock/10,000 (MSB) | TBD | TBD | TBD |
| | 4A | Horizontal Active = xxxx pixels (lower 8 bits) | TBD | TBD | TBD |
| | 4B | Horizontal Blanking (Thbp) = xxxx pixels (lower 8 bits) | TBD | TBD | TBD |
| | 4C | Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits) | TBD | TBD | TBD |
| | 4D | Vertical Active = xxxx lines | TBD | TBD | TBD |
| | 4E | Vertical Blanking (Tvbp) = xxxx lines (DE Blanking typ. for DE only panels) | TBD | TBD | TBD |
| | 4F | Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits) | TBD | TBD | TBD |
| | 50 | Horizontal Sync, Offset (Thfp) = xxxx pixels | TBD | TBD | TBD |
| | 51 | Horizontal Sync, Pulse Width = xxxx pixels | TBD | TBD | TBD |
| | 52 | Vertical Sync, Offset (Tvfp) = xx lines Sync Width = xx lines | TBD | TBD | TBD |
| | 53 | Horizontal Vertical Sync Offset/Width upper 2 bits | TBD | TBD | TBD |
| | 54 | Horizontal Image Size =xxx mm | TBD | TBD | TBD |
| | 55 | Vertical image Size = xxx mm | TBD | TBD | TBD |
| | 56 | Horizontal Image Size / Vertical image size | TBD | TBD | TBD |
| | 57 | Horizontal Border = 0 (Zero for Notebook LCD) | TBD | TBD | TBD |
| | 58 | Vertical Border = 0 (Zero for Notebook LCD) | TBD | TBD | TBD |
| | 59 | Bit[7] 0 : Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] : The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see VESA EDID Spec 1.3 Bit[0] : See VESA EDID Spec 1.3 ==> fix=1A | TBD | TBD | TBD |
| Timing Descriptor #3 Dell specific information | 5A | Flag | TBD | TBD | TBD |
| | 5B | Flag | TBD | TBD | TBD |
| | 5C | Flag | TBD | TBD | TBD |
| | 5D | Data Type Tag: Alphanumeric Data String (ASCII) ==> fix=FE | TBD | TBD | TBD |
| | 5E | Flag | TBD | TBD | TBD |
| | 5F | Dell P/N 1 st Character | TBD | TBD | TBD |
| | 60 | Dell P/N 2 nd Character | TBD | TBD | TBD |
| | 61 | Dell P/N 3 rd Character | TBD | TBD | TBD |



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| | | | | | |
|----------------------|----------------------------------|--|-----|-----|-----|
| | 62 | Dell P/N 4 th Character | TBD | TBD | TBD |
| | 63 | Dell P/N 5 th Character | TBD | TBD | TBD |
| | EDID Revision | | | | |
| | Bit[6:0] See charts below | | | | |
| | 64 | Bit[7] 0: X-rev, 1: A-rev | TBD | TBD | TBD |
| | 65 | Manufacturer P/N | TBD | TBD | TBD |
| | 66 | Manufacturer P/N | TBD | TBD | TBD |
| | 67 | Manufacturer P/N | TBD | TBD | TBD |
| | 68 | Manufacturer P/N | TBD | TBD | TBD |
| | 69 | Manufacturer P/N | TBD | TBD | TBD |
| | 6A | Manufacturer P/N | TBD | TBD | TBD |
| Timing Descriptor #4 | 6B | Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h) | TBD | TBD | TBD |
| | 6C | Flag | TBD | TBD | TBD |
| | 6D | Flag | TBD | TBD | TBD |
| | 6E | Flag | TBD | TBD | TBD |
| | 6F | Data Type Tag: Manufacturer Specified Data 00 ==>fix=00 | TBD | TBD | TBD |
| | 70 | Flag | TBD | TBD | TBD |
| | 71 | Color Management | TBD | TBD | TBD |
| | 72 | Panel Structure | TBD | TBD | TBD |
| | 73 | Frame Rate | TBD | TBD | TBD |
| | 74 | Light Controller Interface and Luminance | TBD | TBD | TBD |
| | 75 | Outdoor Features | TBD | TBD | TBD |
| | 76 | Multi-Media Features | TBD | TBD | TBD |
| | 77 | Multi-Media Features | TBD | TBD | TBD |
| | 78 | Special Features #1 | TBD | TBD | TBD |
| | 79 | Special Features #2 | TBD | TBD | TBD |
| | 7A | Special Features #3 | TBD | TBD | TBD |
| | 7B | (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h) | TBD | TBD | TBD |
| | 7C | (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h) | TBD | TBD | TBD |
| | 7D | (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h) | TBD | TBD | TBD |
| Checksum | 7E | Extension flag (# of optional 128 EDID extension blocks to follow, Typ = 0) | TBD | TBD | TBD |
| | 7F | Checksum (The 1-byte sum of all 128 bytes in this EDID block shall = 0) | TBD | TBD | TBD |